DECLARATION

I, the undersigned, of 2-12, Nakazaki 2-chome, Kita-ku, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **8-296592**

that was filed in Japanese.

I declare that all statements made herein of may own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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(Translation)

[Name of the Document] SPECIFICATION

[Title of the Invention] Semiconductor device and method and apparatus for fabricating the same

[Claims]

[Claim 1] A method for fabricating a semiconductor device, characterized by comprising the steps of:

forming a semiconductor wafer having a first semiconductor region, to be a part of a semiconductor element, and a second semiconductor region for optical monitoring;

monitoring optical properties of the second semiconductor region;

performing an etching process on the first and the second semiconductor regions simultaneously; and

controlling conditions for the etching process based on the optical properties in the second semiconductor region.

[Claim 2] The method for fabricating a semiconductor device of Claim 1, characterized in that the step of monitoring optical properties comprises the steps of:

irradiating measurement light onto the second semiconductor region;

intermittently irradiating exciting light onto the second semiconductor region; and

calculating, as a variation amount of a reflectivity, a value obtained by dividing a difference in reflectivity of the measurement light from the second semiconductor region depending upon whether or not the exciting light has been irradiated onto the second semiconductor region by a reflectivity of the measurement light from the second semiconductor region in the case where the exciting light has not been irradiated onto the second semiconductor region.

[Claim 3] The method for fabricating a semiconductor device of Claim 1,

characterized in that dry etching using plasma is performed in the step of performing an etching process.

[Claim 4] The method for fabricating a semiconductor device of Claim 1, further comprising the steps of:

depositing an interlevel insulating film on the first semiconductor region and the second semiconductor region on the semiconductor wafer; and

selectively removing the interlevel insulating film to form a first opening reaching the first semiconductor region and a second opening reaching the second semiconductor region,

characterized in that, in the step of etching the first and the second semiconductor regions, light dry etching for removing a damaged layer formed in the vicinity of a surface,

through which the first and the second semiconductor regions are exposed with the openings formed, is performed,

and that, in the step of monitoring the optical properties, initial optical properties of the second semiconductor region, before the interlevel insulating film has been formed, are detected beforehand and the optical properties of the second semiconductor region, after the opening has been formed, are monitored,

and that, in the step of controlling the conditions for an etching process,

the initial optical properties and the optical properties of the second semiconductor region, which vary as the etching proceeds, are compared with each other, thereby controlling the conditions for the etching process.

[Claim 5] The method for fabricating a semiconductor device of Claim 4, characterized in that the step of monitoring the optical properties comprises the steps of:

irradiating measurement light onto the second semiconductor region;

intermittently irradiating exciting light onto the second semiconductor region; and

calculating, as a variation amount of a reflectivity, a value obtained by dividing a difference in reflectivity of the measurement light from the second semiconductor region depend-

ing upon whether or not the exciting light has been irradiated onto the second semiconductor region by a reflectivity of the measurement light from the second semiconductor region in the case where the exciting light has not been irradiated onto the second semiconductor region,

and that, in the step of controlling the conditions for the etching process, the time of the etching process is controlled such that the light dry etching is performed until the variation amount of the reflectivity reaches a predetermined value.

[Claim 6] The method for fabricating a semiconductor device of Claim 1, 2, 3, 4 or 5,

characterized in that a wavelength range of the measurement light is equal to or shorter than 600 nm.

[Claim 7] The method for fabricating a semiconductor device of Claim 1, 2, 3, 4, 5 or 6,

characterized in that, in the step of forming a semiconductor wafer, the second semiconductor region is provided in a region different from a region within the semiconductor wafer, in which a semiconductor chip, including the semiconductor element, is formed.

[Claim 8] The method for fabricating a semiconductor device of Claim 1, 2, 3, 4, 5 or 6,

characterized in that, in the step of forming a semiconductor wafer, the second region is provided in a region within

the semiconductor wafer, in which a semiconductor chip, including the semiconductor element, is formed.

[Claim 9] The method for fabricating a semiconductor device of Claim 1, 2, 3, 4, 5, 6, 7 or 8,

characterized in that, in the step of forming a semiconductor wafer, the first and the second semiconductor regions are made of n-type silicon single crystals.

[Claim 10] An apparatus for fabricating a semiconductor device characterized by comprising:

a chamber for disposing a semiconductor device therein and processing the semiconductor device;

processing means for performing an etching process on the semiconductor device in the chamber;

first light incidence means for intermittently irradiating exciting light onto the semiconductor device disposed in the chamber;

second light incidence means for irradiating measurement light onto the semiconductor device disposed in the chamber;

reflectivity detection means for detecting a reflectivity of the measurement light irradiated onto the semiconductor device;

variation calculation means for receiving an output of the reflectivity detection means and calculating a variation of the reflectivity of the measurement light depending upon whether or

not the exciting light has been irradiated from the first light incidence means; and

process control means for receiving an output of the variation calculation means and controlling conditions for the etching process based on the variation of the reflectivity.

[Claim 11] The apparatus for fabricating a semiconductor device of Claim 10,

characterized in that the processing means generates plasma in the chamber and thereby performs etching on the semiconductor device.

[Claim 12] The apparatus for fabricating a semiconductor device of Claim 10,

characterized in that the first and the second light incidence means are configured such that an incidence angle of the measurement light onto an upper surface of the semiconductor device becomes larger than an incidence angle of the exciting light onto the upper surface of the semiconductor device.

[Claim 13] A semiconductor device characterized by comprising:

a semiconductor wafer;

a first region which is provided on the semiconductor wafer and is to be a part of a semiconductor element to be formed on the semiconductor wafer; and

a second region for monitoring optical properties in the first region during processing thereof.

[Claim 14] The semiconductor device of Claim 13,

characterized in that the second region is provided in a region different from a region, in which a semiconductor chip, including the semiconductor element, is formed.

[Claim 15] The semiconductor device of Claim 13,

characterized in that the second region is provided in a region, in which a semiconductor chip, including the semiconductor element, is formed.

[Claim 16] The semiconductor device of Claim 13, 14 or 15,

characterized in that the second region is a region, which is made of a semiconductor material and is used for measuring a reflectivity of light.

[Claim 17] The semiconductor device of Claim 16,

characterized in that the first and the second regions are made of n-type silicon single crystals.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor device and a method and an apparatus for fabricating the same, and more particularly relates to improving the control of the characteristics of a semiconductor device during the fabrication process thereof.

[0002]

[Prior Art]

In recent years, semiconductor integrated circuits have achieved a remarkably high degree of integration. Thus, in a MOS type semiconductor device, efforts have also been made in order to develop a transistor device having an even smaller size and an even higher performance. Now that a transistor device of such a very small size has been provided, it is particularly necessary to realize a highly reliable MOS device. In order to improve the reliability of a MOS device, each portion constituting the MOS device is required to have high reliability.

[0003]

For example, the reliability of a contact portion, which is affected by a method for forming a contact window, is an important factor determining the reliability of such a MOS device. A damaged layer of a semiconductor substrate, which is produced by dry etching used for forming the contact window, is removed by wet etching subsequent to the dry etching. In order to appropriately determine the amount of removal, a monitor wafer or the like has conventionally been used for measuring the electric characteristics thereof, thereby sensing the depth and the like of the damaged layer produced under the dry-etching conditions. And various conditions, including duration, temperature and the like, are set for the wet etching intended to remove the damaged layer. Thus, the conventional method for fabricating a semiconductor device performs a control so as to optimize the processing conditions during the fabricating process of the

semiconductor device based on the electrical characteristics obtained by using the monitor wafer.

[0004]

[Problems to be Solved by the Invention]

By the way, as the size of a MOS device has been reduced in the above-described manner, the planar size (the lateral size) of a contact window has also been reduced, whereas the depth of the contact window has not been reduced. As a result, the aspect ratio (= depth/lateral size) is rather increased. And, in order to form such a contact window having a high aspect ratio, high-vacuum/high-density plasma has been used in a dry-etching process, for example. The high-vacuum/high-density plasma process has realized the formation of a deep contact window by using ions having high energy in satisfactorily aligned directions. However, the depth of the damaged layer, which is produced in semiconductor crystals on the bottom of a contact, and the degree of the damage have been increased by the impact of the ions having high energy, as compared with the level of the defects which have been produced by a conventional dry etching process using relatively low-vacuum/low-density plasma.

[0005]

Thus, it is now difficult to ensure the removal of the damaged layer or to remove the damaged layer with satisfactory controllability only by using the conventional method for fab-

ricating a semiconductor device without applying any modification thereto.

[0006]

The above-described points are also true of various kinds of processing other than the etching process. Thus, a process and a control method, which can precisely and rapidly sense the states of various factors affecting the characteristics of a semiconductor device and which can realize desired characteristics for the semiconductor device with satisfactory reproducibility, are earnestly demanded.

[0007]

In view of these respects, the present invention has been devised and the objectives thereof are providing a structure for a semiconductor device which can realize satisfactory and uniform characteristics by surely sensing in-line the factors causing the degradation in reliability of the semiconductor device and doing damage thereon during the fabrication process thereof, and providing a method and an apparatus for fabricating such a semiconductor device.

[0008]

[Means for Solving the Problems]

In order to accomplish the above-described objectives, the present invention takes various means regarding a method for fabricating a semiconductor device which are recited in Claims 1 to 9, various means regarding an apparatus for fabricating a semiconductor device which are recited in Claims 10 to 12, and

various means regarding a semiconductor device which are recited in Claims 13 to 17.

[0009]

As recited in Claim 1, the first method for fabricating a semiconductor device of the present invention includes the steps of: forming a semiconductor wafer having a first semiconductor region, to be a part of a semiconductor element, and a second semiconductor region for optical monitoring; monitoring optical properties of the second semiconductor region; performing an etching process on the first and the second semiconductor regions simultaneously; and controlling conditions for the etching process based on the optical properties in the second semiconductor region.

[0010]

This makes it possible to detect the depth of a damaged layer, which is caused by etching in the first semiconductor region during an etching process of a semiconductor device, and the degree of the damage from the optical properties of the second semiconductor region. Thus, as compared with a conventional fabrication method in which the electrical characteristics are detected after an etching process is completed and then fed back to the etching conditions, the characteristics of the semiconductor device can be controlled to obtain desired values with higher precision and smaller variation.

[0011]

As recited in Claim 2, the step of monitoring the optical properties of Claim 1 may include the steps of: irradiating measurement light onto the second semiconductor region; intermittently irradiating exciting light onto the second semiconductor region; and calculating, as a variation of a reflectivity, a value obtained by dividing a difference in reflectivity of the measurement light from the second semiconductor region depending upon whether or not the exciting light has been irradiated onto the second semiconductor region by a reflectivity of the measurement light from the second semiconductor region in the case where the exciting light has not been irradiated onto the second semiconductor region.

[0012]

In such a case, if the exciting light is irradiated onto the second semiconductor region, then the carriers are excited, and the electric field is varied in accordance with the variation in numbers of the carriers. As a result, the reflectivity of the exciting light is varied. And, the period during which the carriers are in an excited state has certain longevity. The longevity is shortened if a large number of defects exist in the second semiconductor region, because the carriers are trapped by the defects. And, since the longevity of the carriers is shortened, the electric field formed by the carriers becomes small and the increase in reflectivity of the measurement light is attenuated. Thus, by monitoring the variation of the reflectivity, the depth of a damaged layer and the degree

of the damage can be detected and control can be performed to obtain appropriate etching conditions.

[0013]

As recited in Claim 3, dry etching using plasma may be performed in the step of performing an etching process of Claim 1.

[0014]

This makes it possible to detect the degree of the damage, which is caused in the first semiconductor region owing to the impact of the ions during plasma processing, while monitoring the second semiconductor region. Thus, a semiconductor device having satisfactory characteristics can be formed by a process using plasma, which is universally employed for the fabrication processes of a semiconductor device.

[0015]

As recited in Claim 4, the second method for fabricating a semiconductor device of the present invention further includes, in addition to those of Claim 1, the steps of: depositing an interlevel insulating film on the first semiconductor region and the second semiconductor region on the semiconductor wafer; and selectively removing the interlevel insulating film to form a first opening reaching the first semiconductor region and a second opening reaching the second semiconductor region. In the step of etching the first and the second semiconductor regions, light dry etching for removing a damaged layer formed in the vicinity of a surface, through which the first and the second semiconductor regions are exposed with the openings formed,

is performed. In the step of monitoring the optical properties, initial optical properties of the second semiconductor region, before the interlevel insulating film has been formed, are detected beforehand and the optical properties of the second semiconductor region, after the respective openings have been formed, are monitored. In the step of controlling the conditions for etching process, the initial optical properties and the optical properties of the second semiconductor region, which vary as the etching proceeds, are compared with each other, thereby controlling the conditions for the etching process.

[0016]

This makes it possible to suppress the generation of a new damage owing to excessive light dry etching, while surely removing the damaged layer which is formed in the first semiconductor region when the first opening, functioning as a contact hole of the semiconductor device, is formed.

[0017]

As recited in Claim 5, the step of monitoring the optical properties of Claim 4 may include the steps of: irradiating measurement light onto the second semiconductor region; intermittently irradiating exciting light onto the second semiconductor region; and calculating, as a variation of a reflectivity, a value obtained by dividing a difference in reflectivity of the measurement light from the second semiconductor region depending upon whether or not the exciting light

has been irradiated onto the second semiconductor region by a reflectivity of the measurement light from the second semiconductor region in the case where the exciting light has not been irradiated onto the second semiconductor region. In the step of controlling the conditions for the etching process, the time of the etching process can be controlled such that the light dry etching is performed until the variation amount of the reflectivity reaches a predetermined value.

[0018]

This makes it possible to attain the same effects as those of Claim 2.

[0019]

As recited in Claim 6, a wavelength range of the measurement light is preferably equal to or shorter than 600 nm in Claim 1, 2, 3, 4 or 5.

[0020]

As recited in Claim 7, in the step of forming a semiconductor wafer, the second semiconductor region may be provided in a region different from a region within the semiconductor wafer, in which a semiconductor chip, including the semiconductor element, is formed in Claim 1, 2, 3, 4, 5 or 6. Alternatively, as recited in Claim 8, the second semiconductor region may also be provided in a region in which a semiconductor chip, including the semiconductor element, is formed.

[0021]

As recited in Claim 9, in the step of forming a semiconductor wafer, the first and the second semiconductor regions are preferably made of n-type silicon single crystals in Claim 1, 2, 3, 4, 5, 6, 7 or 8.

[0022]

As recited in Claim 10, the apparatus for fabricating a semiconductor device of the present invention includes: a chamber for disposing a semiconductor device therein and processing the semiconductor device; processing means for performing an etching process on the semiconductor device in the chamber; first light incidence means for intermittently irradiating exciting light onto the semiconductor device disposed in the chamber; second light incidence means for irradiating measurement light onto the semiconductor device disposed in the chamber; reflectivity detection means for detecting a reflectivity of the measurement light irradiated onto the semiconductor device; variation calculation means for receiving an output of the reflectivity detection means and calculating a variation of the reflectivity of the measurement light depending upon whether or not the exciting light has been irradiated from the first light incidence means; and process control means for receiving an output of the variation calculation means and controlling conditions for the etching process based on the variation of the reflectivity.

[0023]

By using this apparatus for fabricating a semiconductor device, the method for fabricating a semiconductor device as recited in Claim 2 or 4 can be implemented easily. That is to say, by monitoring the variation amount of the reflectivity of the measurement light, an apparatus for fabricating a semiconductor device, which can fabricate a semiconductor device having desired characteristics with a satisfactory reproducibility, is obtained.

[0024]

As recited in Claim 11, the processing means of Claim 10 may be means for generating plasma in the chamber and thereby performing etching on the semiconductor device.

[0025]

As recited in Claim 12, the first and the second light incidence means of Claim 10 are preferably configured such that an incidence angle of the measurement light onto an upper surface of the semiconductor device becomes larger than an incidence angle of the exciting light onto the upper surface of the semiconductor device.

[0026]

This makes it possible to irradiate the measurement light, using the reflected light, onto a narrow region and to reduce the area of the second semiconductor region.

[0027]

As recited in Claim 13, the semiconductor device of the present invention includes: a semiconductor wafer; a first re-

gion which is provided on the semiconductor wafer and is to be a part of a semiconductor element to be formed on the semiconductor wafer; and a second region for monitoring optical properties of the first region during processing thereof.

[0028]

This makes it possible to monitor the states of the first region, which are variable in accordance with the process proceeding situations in the first region when a semiconductor wafer is subjected to various types of processing, while utilizing the optical properties of the second region. As a result, a semiconductor device, having a configuration allowing for appropriately determining the processing conditions, the processing time and the like in wide variety of processing, can be obtained.

[0029]

As recited in Claim 14, the second region may be provided in a region different from a region, in which a semiconductor chip, including the semiconductor element, is formed in Claim 13. Alternatively, as recited in Claim 15, the second region may also be provided in a region in which a semiconductor chip, including the semiconductor element, is formed.

[0030]

As recited in Claim 16, the second region may be a region, which is made of a semiconductor material and is used for measuring a reflectivity of light in Claim 13, 14 or 15.

[0031]

This makes it possible to obtain a semiconductor wafer, which can be used in the method for fabricating a semiconductor device as recited in Claim 2 or 4.

[0032]

As recited in Claim 17, the first and the second regions are preferably made of n-type silicon single crystals in Claim 16.

[0033]

[Embodiments of the Invention]

Hereinafter, embodiments of the present invention will be described.

[0034]

First, a method for fabricating a semiconductor device, the cross-sectional structure and the planar structure thereof according to this embodiment will be described with reference to Figures **1** to **3**. Figure **1** is a flow chart illustrating a method for fabricating a semiconductor wafer according to this embodiment. On the other hand, Figures **2(a)** through **2(c)** are cross-sectional views of a silicon wafer illustrating the process steps for fabricating the semiconductor device according to this embodiment. Furthermore, Figure **3** is a top view schematically showing the structure of the silicon wafer according to the embodiment.

[0035]

As shown in Figure **3**, a chip region **Rtp** to be a semiconductor chip finally by being cut out of a wafer, and a monitor

region **Rmn** for optical evaluation are provided on a p-type silicon wafer **103**.

[0036]

And, prior to the step illustrated in Figure **2(a)**, an n-type semiconductor region (the specific resistance of which is about 0.02 Ωcm) **101** having an area of 13×13 mm^2, for example, has been formed in the monitor region **Rmn** on the silicon wafer **103**. On the other hand, various semiconductor elements have been formed in the chip region **Rtp**. In Figure **2(a)**, a MOS transistor including: a gate electrode **106** made of poly-silicon; a gate oxide film **107** having a thickness of 6 nm, for example; an n-type source region **108**; and an n-type drain region **109**, is shown as an example thereof. And, an interlevel insulating film **104** is deposited over the entire surface of the wafer. In this embodiment, the n-type semiconductor region **101** is doped an impurity having the same conductivity type and the same concentration as those of the n-type source region **108** and the n-type drain region **109**. However, as will be described later, an impurity having a different conductivity type and a different concentration from those of the source/drain regions of the semiconductor element to be monitored may be doped into the semiconductor region in the monitor region **Rmn**.

[0037]

Next, in the step illustrated in Figure **2(b)**, a photoresist mask **105** for forming contact holes is formed on the interlevel

insulating film **104**. Dry etching is performed in order to selectively remove the interlevel insulating film **104** by using the photoresist mask **105**. As will be described later, the dry etching is a process using plasma. The etching conditions are, for example, as follows. A mixed gas of Ar gas, CHF_3 gas and CF_4 gas is used. The flow rate of the Ar gas is 80 sccm, that of the CHF_3 gas is 45 sccm, and that of the CF_4 gas is 20 sccm. The overall gas pressure is set at 80 mTorr to cause radio frequency discharge with a power of 400 W. By this dry-etching process, not only the openings **110a** and **110b** which are contact holes respectively reaching the n-type source region **108** and the n-type drain region **109** of the MOS transistor, but also an opening for monitoring **110c** reaching the n-type semiconductor region **101** are formed. And, at a point in time when the completion of the formation of the respective openings **110a** to **110c** by the plasma luminescence method is detected, damaged layers **Rdm1**, **Rdm2** and **Rdm3** have respectively been formed in the n-type source region **108**, the n-type drain region **109**, and the n-type semiconductor region **101** on the silicon wafer.

[0038]

Next, in the step illustrated in Figure **2(c)**, light etching (dry etching) is performed in order to remove the damaged layers **Rdm1** to **Rdm3** resulting from the dry etching. In this step, the present embodiment applies the conditions where the gas flow rates and pressure are not changed and the power is reduced to 200 W.

[0039]

Figure **1** is a flow chart showing a procedure of the optical monitoring.

[0040]

First, in Step **ST1**, the initial variation amount of reflection intensity in the n-type semiconductor region **101** before the interlevel insulating film **104** has been deposited, is measured. Herein, in this embodiment, since the irradiation intensity of the measurement light (in each wavelength region) is assumed to be constant, detecting a reflection intensity is substituted for detecting a reflectivity. The measurement of the variation amount of the reflection intensity is performed by continuously irradiating Xe lamp light (probe light) **403** from another direction while intermittently irradiating the n-type semiconductor region **101** with Ar ion laser light (exciting light) **402**, and then by detecting the variation in reflection intensity of the probe light **403**. That is to say, a value (**ΔR/R**) obtained by dividing a difference **ΔR** between the reflection intensity when the n-type semiconductor region **101** is irradiated with the Ar ion laser light **402** and the reflection intensity when it is not irradiated with the Ar ion laser light **402** by the reflection intensity **R** when the n-type semiconductor region **101** is not irradiated with the Ar ion laser light **402** is defined as the variation amount of reflection intensity.

[0041]

Herein, it is considered that such a variation amount (**Δ R/R**) of reflection intensity results from the following action. In general, when semiconductor is irradiated with light, carriers are excited by the light to increase the number thereof. Thereafter, when the carriers return to the original energy level, they are extinct while emitting light. An electric field is varied in accordance with such a variation in numbers of carriers. Thus, the reflection intensity when exciting light is irradiated is different from the reflection intensity when exciting light is not irradiated. However, if a large number of defects exist in the semiconductor, then interface states at lower energy levels come to exist owing to the defects. And the defects having such interface states function as a carrier-trapping layer. Thus, if the carriers are trapped by the defects so as not to be excited to sufficiently high energy levels even by the irradiation of light, or if the carriers, which have been excited to high energy levels, are trapped by the defects, then the intensity of the light, emitted when the excited carriers return to the low energy levels, is decreased. As a result, the electric field is also varied. Accordingly, the variation amount (**Δ R/R**) of reflection intensity becomes smaller as the depth of a damaged layer and the degree of damage become larger. Thus, information about the damaged layer can be obtained by monitoring the variation amount of reflection intensity.

[0042]

Next, plasma processing is performed in Step **ST102**, and the variation amount (**Δ R/R**) of reflection intensity is monitored in Step **ST103**. Further, in Step **ST104**, it is determined whether or not the removal of the damaged layer has been completed, while comparing the increment amount rate (**Δ R/R**) of the reflection intensity with the initial value. The processing in Steps **ST102** to **ST104** is repeatedly performed until the removal of the damaged layer is completed. When the removal of the damaged layer is completed, the plasma processing is terminated in Step **ST105**.

[0043]

Figure **4** is a cross-sectional view schematically showing the configuration of an etching apparatus including means for observing a reflection intensity **R**. As shown in this figure, an anode electrode **213** functioning as a lower electrode and a cathode electrode **214** functioning as an upper electrode are provided in a reaction-processing chamber **200**. A p-type silicon wafer **103** is placed as an object to be processed on the anode electrode **213**. And it is configured such that when radio frequency power is supplied from a radio frequency power supply **211** to between the two electrodes **213** and **214** via a coupling capacitor **212**, plasma **401** is generated in the reaction-processing chamber **200**. Additionally, a window for detecting an end-point **215**, a window for making probe light incident **218** and a window for observing reflected light **219** are provided in the wall faces of the reaction-processing chamber **200**.

[0044]

On the other hand, an end-point detection system **216** and a member for observing the reflection intensity **R** are provided outside of the reaction-processing chamber **200**. First, a Xe lamp **302** for generating probe light (wavelength: 376 nm, energy: 3.3 eV) to be irradiated onto the n-type semiconductor region **101** is provided. The incident probe light **403** generated by the Xe lamp **302** is reflected by a mirror **217** and is provided through the window for making probe light incident **218** onto the n-type semiconductor region **101** on the wafer **213** disposed in the reaction-processing chamber **200**. And, the light **404** reflected by the n-type semiconductor region **101** (reflected light) is taken out of the reaction-processing chamber **200** through the window for observing reflected light **219**. And, the intensity thereof is detected by a reflection-intensity observation system **220**. Data about the reflection intensity measured by the reflection-intensity observation system **220** is transmitted to an etching control system **222** through a signal path **221**. An Ar ion laser **301** for generating exciting light to be irradiated onto the n-type semiconductor region **101** is also provided. The laser light **402** from the Ar ion laser **301** is chopped by a chopper **223** at a frequency of 200 Hz and is provided intermittently. The laser light **402** is provided into the reaction-processing chamber **200** through the window for detecting an end point **215** and is intermittently irradiated onto the n-type semiconductor region **101**. And, as described above, a value (Δ

R/R) obtained by dividing a difference **ΔR** in reflection intensities, which is caused depending upon whether or not the laser light **402** has been irradiated, by the reflection intensity **R** in the case where it is not irradiated with the laser light **402** is detected by the reflection intensity observation system **220** as the variation amount of reflection intensity. The variation in variation amounts of reflection intensity is monitored by the above-described configuration.

Hereinafter, the relationship between the variation amount of reflection intensity and the state of the damaged layer will be described. Figure **5** is a diagram showing the variation of the ratio of the variation amount of reflection intensity (**Δ R/R**) at a wavelength of 376 nm (energy: 3.3 eV) to the initial value thereof over the time. As shown in Figure **5**, the variation amount of reflection intensity (**Δ R/R**) immediately after the light etching started (between 0 to 20 seconds) is larger than the value when the dry etching is completed in the main step to be closer to the initial value thereof. Thus, it can be understood that the damaged layers have been removed. However, as the light etching time increases (after 20 seconds has passed), the ratio of the variation amount of reflection intensity (**Δ R/R**) to the initial value thereof becomes gradually smaller than the value when the light etching is started (about 0.6 in the example shown in Figure **5**). Thus, it can be understood that the damage done to Si crystals (substrate) is increased by excessive light etching.

[0045]

On the other hand, as shown in Figure **6**, the correlation between the light etching time and the resistance value (contact resistance) of a contact portion can be obtained by performing an experiment beforehand. As shown in Figure **6**, the contact resistance is high on the initial stage of the light etching, because an organic polymer generated by the main etching has been deposited in the vicinity of the bottom face of the contact holes. It can be understood that it is gradually removed by the subsequent light etching. And, as can be seen from the comparison between Figures **6** and **5**, there is a correlation between the contact resistance and the variation amount of reflection intensity (**ΔR/R**). And, from the correlation, it can be understood that the variation amount of reflection intensity (**ΔR/R**) must be a value corresponding to 60% or more of the initial value thereof in order to set the contact resistance at a nominal value (i.e., $50 \pm 5\ \Omega$ when the cross-sectional size of the contact window is 0.6 mm). Thus, by ending the light-etching step at a point in time when the variation amount of reflection intensity (**ΔR/R**) reaches 60%, the generation of new damage, which might be caused by the subsequent light etching, can be suppressed, while substantially removing the damaged layers resulting from the main etching. As a result, a semiconductor device having a satisfactory contact is realized.

[0046]

Figure **7** shows data for comparing the contact resistance of a MOS transistor formed by the light etching of this embodiment to be performed with the optical monitoring for obtaining information about the damaged layers with the contact resistance of a MOS transistor formed by the conventional light etching without such optical monitoring. As shown in this figure, as compared with a conventional method, variations in contact resistance can be suppressed and a semiconductor device having high quality and high reliability can be fabricated by using the method for fabricating an apparatus for fabricating a semiconductor device of this embodiment.

[0047]

In this embodiment, a monitoring region **Rmn** is provided in the semiconductor wafer **103** separately from the chip region **Rtp**. However, the present invention is not limited to such an embodiment. Thus, the same effects as those attained by this embodiment can also be attained even when a pattern for optical evaluation is provided in the chip region **Rtp**.

[0048]

Furthermore, by controlling the variation in variation amounts of reflection intensity (**Δ R/R**) to be caused by a light-etching process within a predetermined time, the abnormality of a device can be sensed rapidly and the trouble of the device can be prevented.

[0049]

In the above-described embodiment, the etching process is to be dry etching using plasma. However, the present invention is not limited to such an embodiment. For example, the present invention is applicable to dry etching using sputtering gas, not plasma, wet etching and the like.

[0050]

Moreover, the present invention is applicable not only to the etching for removing a large damaged layer from a semiconductor region in which the damaged layer exists from the beginning, but also to etching performed when a semiconductor region substantially free from a damaged layer is etched.

[0051]

Furthermore, in the above-described embodiment, the impurity concentration and the depth of the source/drain regions **108, 109**, which are the first semiconductor regions in the chip region **Rtp**, are assumed to be equal to the impurity concentration and the depth of the n-type semiconductor region **101** in the monitoring region **Rmn** which is the second semiconductor region. However, the present invention is not limited to such an embodiment. The impurity concentrations and the conductivity types of the impurity of the first and the second semiconductor regions may be different from each other. This is because, if only an experiment is performed beforehand, the optical properties (contact resistance in the above-described embodiment) in the second semiconductor region for obtaining an appropriate contact resistance in the first semiconductor region can be ex-

pected. For example, it is possible to improve the detection sensitivity of the variation amount of reflection intensity by setting the impurity concentration in the monitoring region **Rmn** at a particularly high value.

[0052]

Furthermore, in this embodiment, the incidence angle of the probe light **403** as the measurement light is smaller than the incidence angle of the laser light **402** as the exciting light as shown in Figure **4**. However, in order to reduce the area of the second semiconductor region to be monitored, it is preferable to increase the incidence angle of the probe light, the reflection intensity of which needs to be measured.

[0053]

[Effects of the Invention]

According to Claims 1 to 9, when the first semiconductor region, which is a part of a semiconductor element, is processed by etching, the optical properties (e.g., a variation in reflection intensities of light) of the second semiconductor region provided on the same semiconductor wafer are monitored, and the conditions for the etching process for the first semiconductor region are controlled in accordance with the optical properties. Thus, it is possible to provide a method for fabricating a semiconductor device which can precisely and uniformly control the characteristics such as a contact resistance.

[0054]

According to Claims 10 to 12, means for making measurement light incident onto a semiconductor device in a chamber, means for making exciting light intermittently incident onto the semiconductor device, means for measuring the reflection intensity of the measurement light and means for monitoring the variation in reflection intensities of the measurement light depending upon whether or not the exciting light has been irradiated are provided for an apparatus for fabricating a semiconductor device. Thus, it is possible to provide an apparatus for fabricating a semiconductor device which can fabricate a semiconductor device having desired characteristics by utilizing a variation in reflection intensities of the measurement light.

[0055]

According to Claims 13 to 17, a first region to be a part of a semiconductor element and a second region for optically monitoring the process in the first region are provided on one and the same semiconductor wafer as a structure for a semiconductor device. Thus, it is possible to provide a semiconductor device having such a configuration as to be able to appropriately determine various processing conditions, including the degree and the time of the processing, for the first region by utilizing the optical properties in the second region.

[Brief Description of the Drawings]

[Figure 1]

A flow-chart diagram illustrating a method for fabricating a semiconductor device according to an embodiment.

[Figure 2]

Cross-sectional views of a semiconductor wafer illustrating the process steps for fabricating a semiconductor device according to the embodiment.

[Figure 3]

A top view of the semiconductor wafer according to the embodiment.

[Figure 4]

A cross-sectional view of a plasma processing apparatus as an apparatus for fabricating the semiconductor device according to the embodiment.

[Figure 5]

A characteristic diagram showing the relationship between an etching time and the variation amount in reflection intensities of probe light in the embodiment.

[Figure 6]

A characteristic diagram showing the relationship between an etching time and a contact resistance in the embodiment.

[Figure 7]

A diagram showing different variations in contact resistance values of the semiconductor devices which have been

formed by using a light etching method of the embodiment and a conventional light etching method, respectively.

[Description of the Reference Numerals]

101 n-type semiconductor region

103 p-type silicon wafer

104 interlevel insulating film

105 photoresist mask

106 gate electrode

107 gate oxide film

108 n-type source region

109 n-type drain region

110a to **110c** opening

200 reaction-processing chamber

211 radio frequency power supply

212 coupling capacitor

213 anode electrode

214 cathode electrode

215 window for detecting end point

216 end-point detection system

217 mirror

218 window for making probe light incident

219 window for observing reflected light

220 reflection-intensity observation system

221 signal path

222 etching control system

223 chopper

301 Ar ion laser

302 Xe lamp

401 plasma

402 laser light

403 incident probe light

404 reflected light

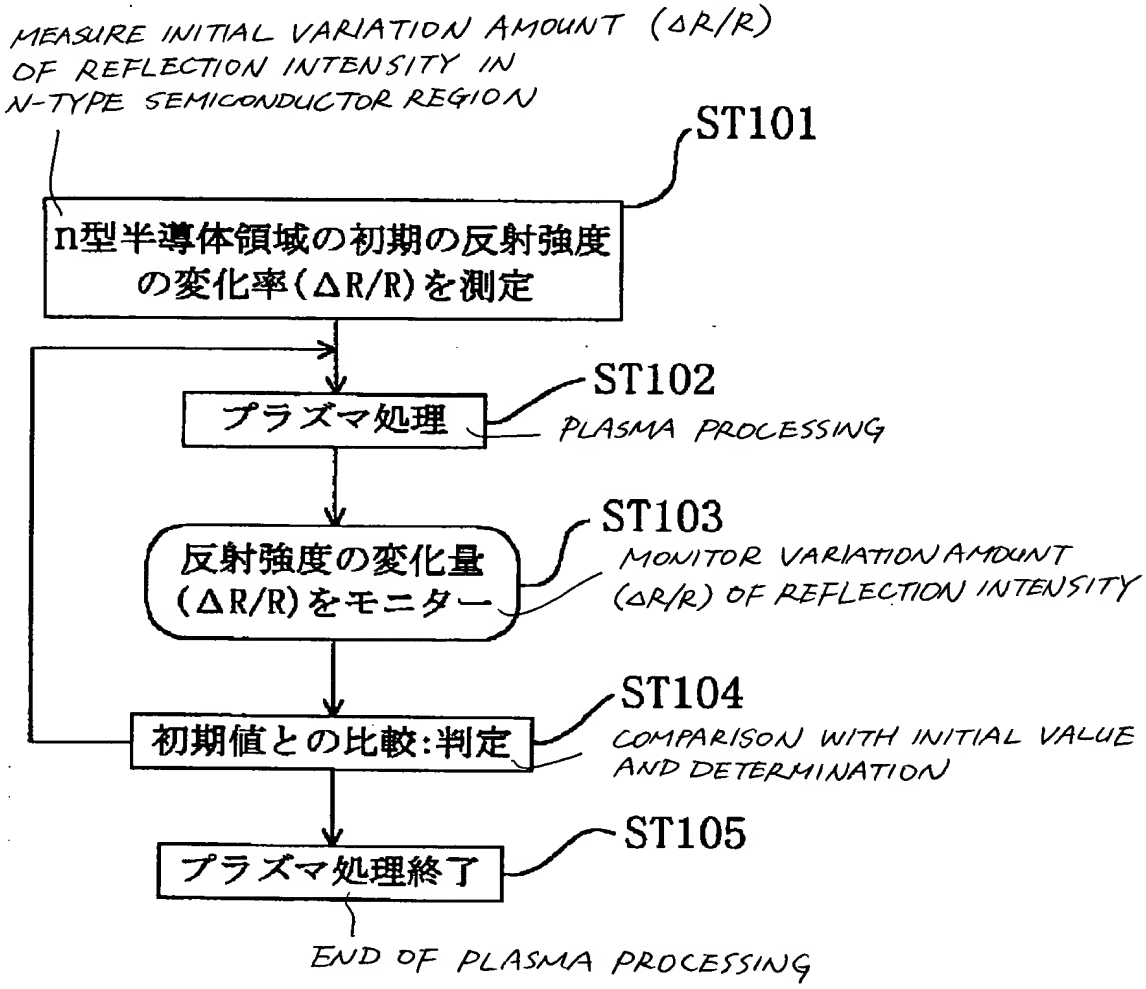
Rtp chip region

Rmn monitoring region

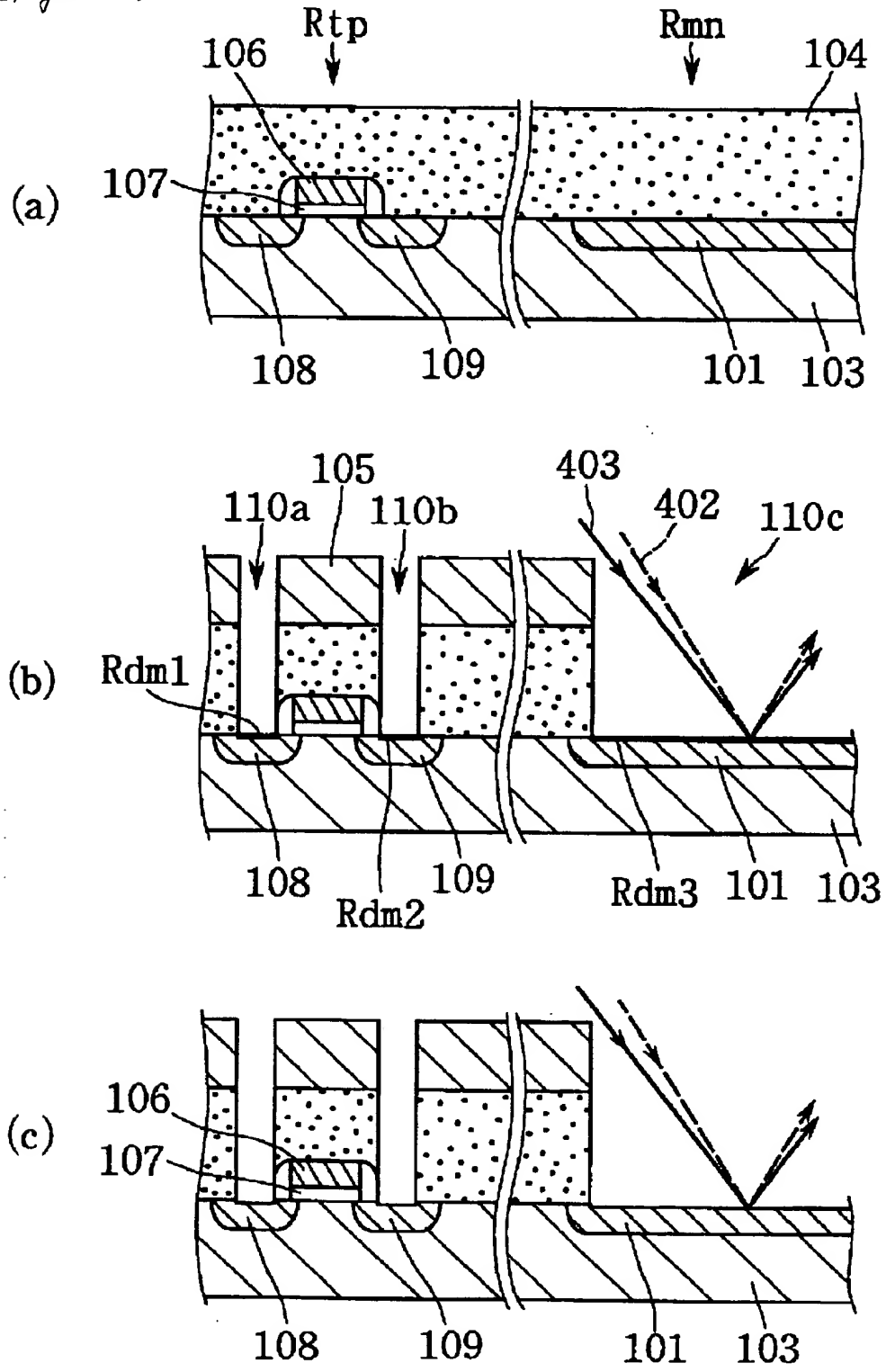
Rdm1 to **Rdm3** damaged layer

【書類名】　図面
[Name of the Document]　DRAWINGS

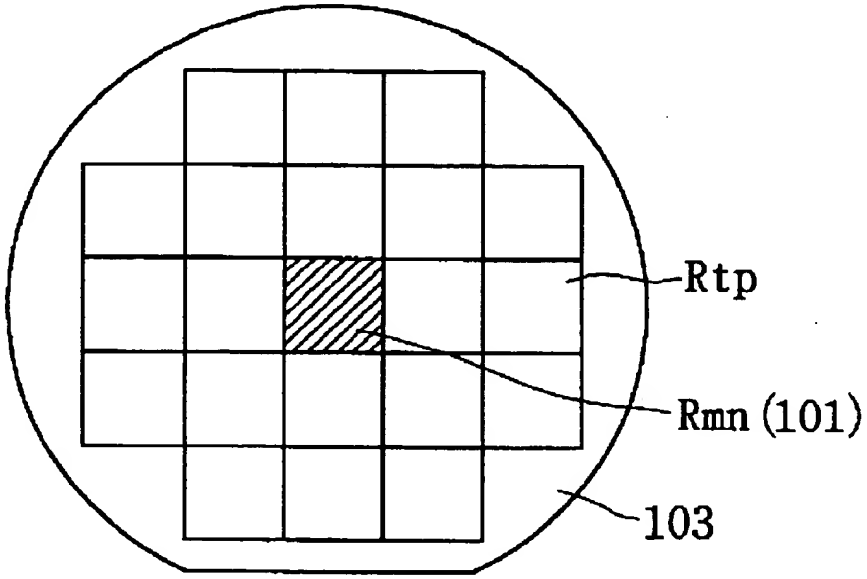
【図１】
[Figure 1]



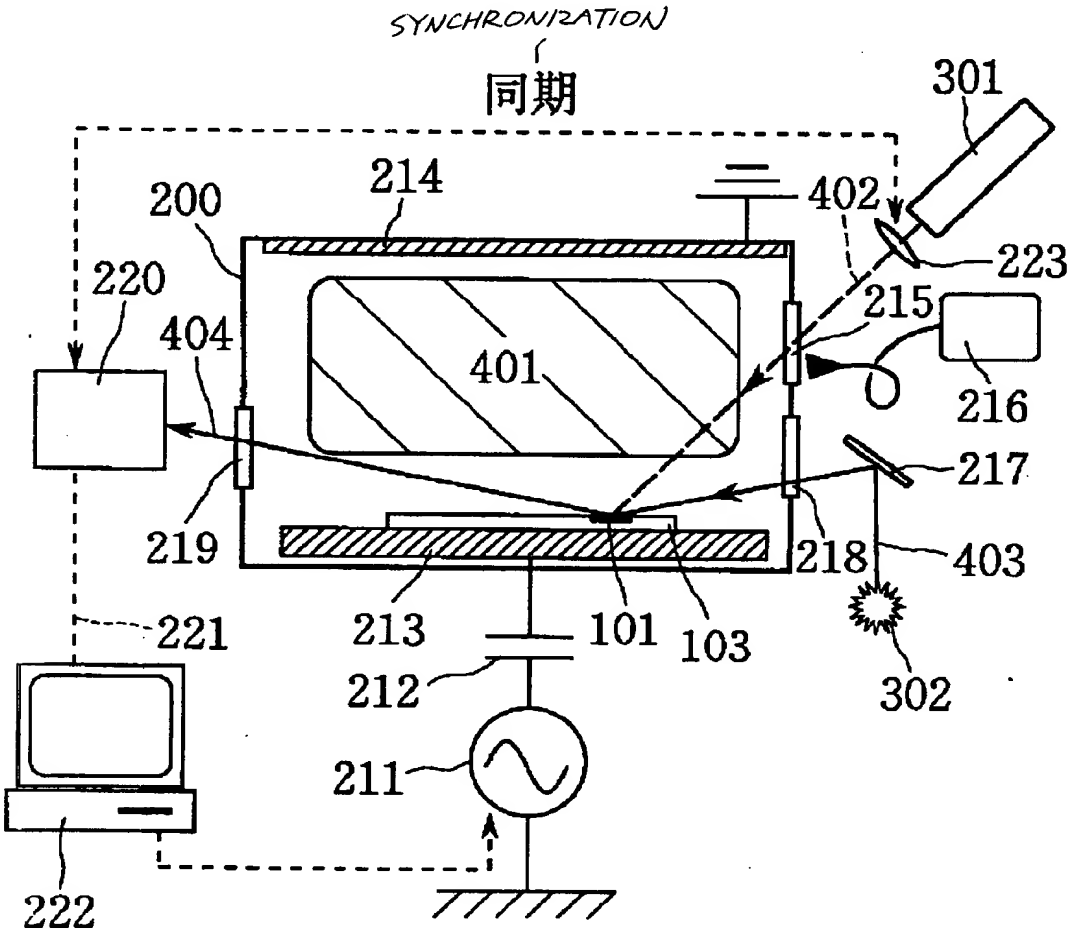
【図２】
[Figure 2]


(a)
Rtp
Rmn
106
104
107
108
109
101
103
(b)
105
403
110a
110b
402
110c
Rdm1
108
Rdm2
109
Rdm3
101
103
(c)
106
107
108
109
101
103

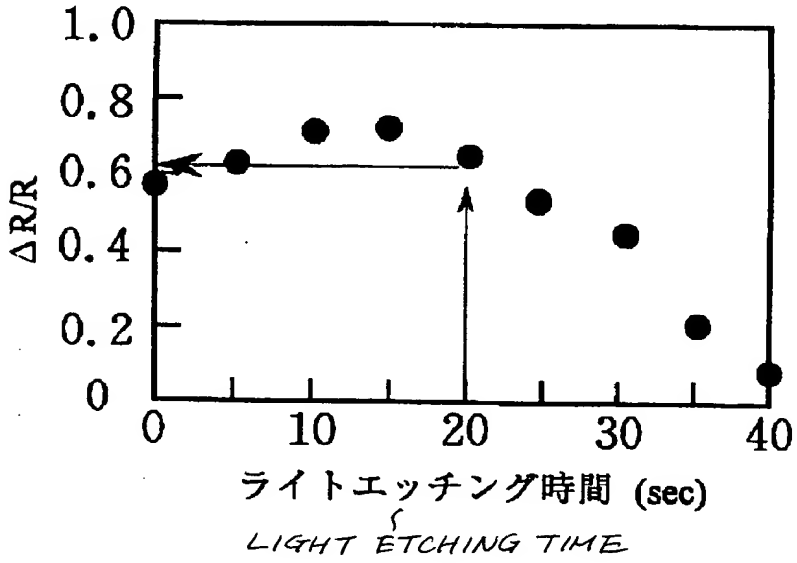
【図３】
[Figure 3]



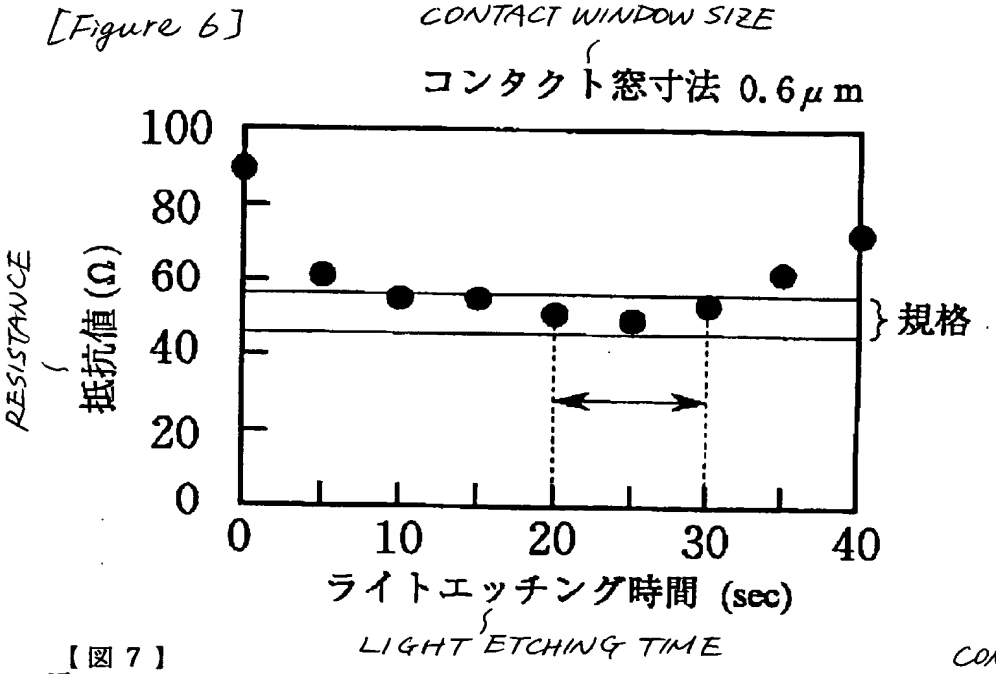
【図４】
[Figure 4]



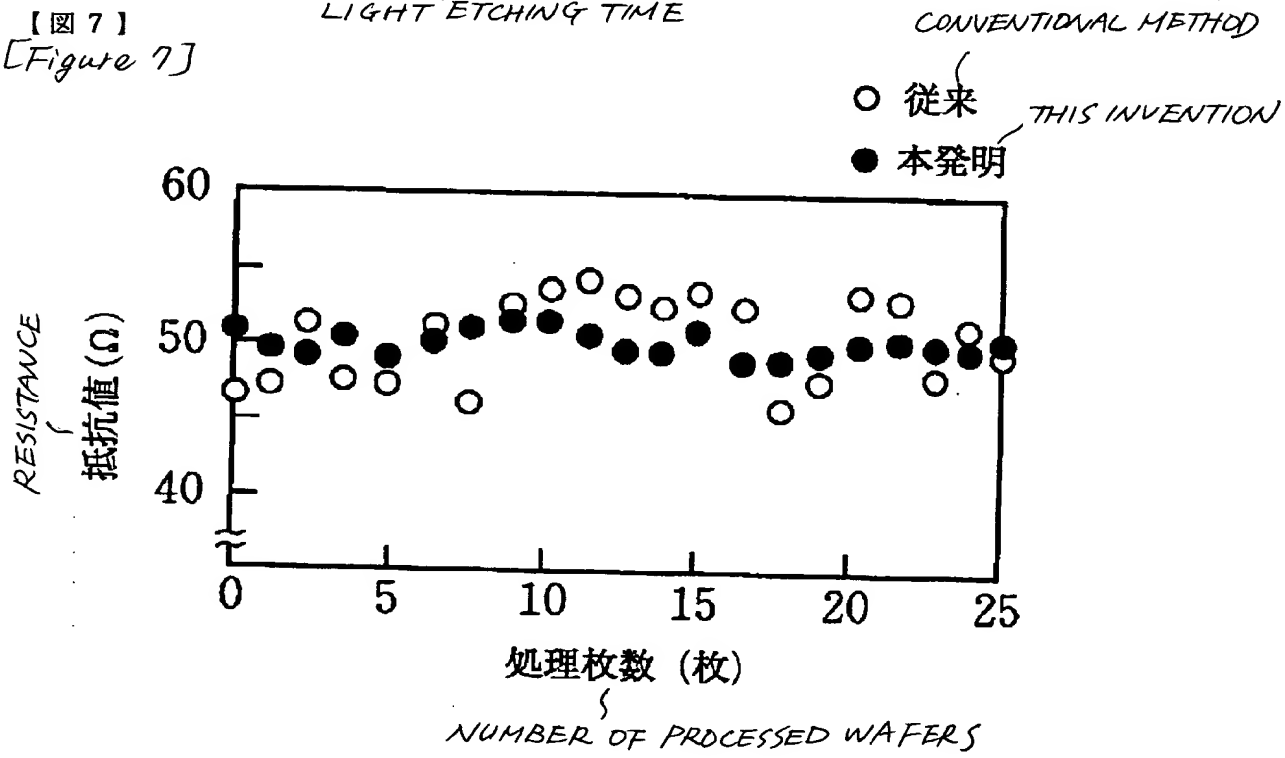
【図５】
[Figure 5]



【図６】
[Figure 6]



【図７】
[Figure 7]



[Name of the Document] ABSTRACT

[Abstract]

[Problem] To provide a semiconductor device and a method and an apparatus for fabricating the same, which can obtain desired characteristics with high precision and can make them consistent by means of an in-line control.

[Means for Solving the Problem] An n-type source region **108**, an n-type drain region **109** and an n-type semiconductor region **101** are provided on a semiconductor wafer **103**. An interlevel insulating film **104**, which has been deposited on the semiconductor wafer **103**, is subjected to dry etching using plasma, thereby forming openings **110a** to **110c** reaching the regions **108**, **109** and **110**, respectively. Thereafter, light etching for removing a damaged layer is performed. During the process, the n-type semiconductor region **101** is intermittently irradiated with exciting laser light **402** and the variation amount of the reflection intensity of probe light **403** depending upon whether or not it has been irradiated with the laser light **402** is monitored, thereby detecting the degree of progress of the removal of the damaged layer and the degree of generation of a new damaged layer and forming a semiconductor device having a small and uniform contact resistance.

[Selected Figure] Figure **2**